WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

a high speed bus interface to interface to a core chipset through a high speed bus;

a serial mass data storage host adapter in communication with the high speed bus interface to control a high speed mass data storage unit; and

a network controller in communication with the high speed bus interface to control a network port.

2. The integrated circuit of Claim 1 wherein the serial mass data storage host adapter is a serial ATA host adapter.

3. The integrated circuit of Claim 1 wherein the serial mass data storage host adapter controls the high speed mass data storage unit in response to a signal from the core chipset.

4. The integrated circuit of Claim 1 wherein the network controller includes an Ethernet controller having an operating speed of at least 1 Giga Bit per second.

5. The integrated circuit of Claim 4 wherein the Ethernet controller includes a MAC layer and a physical layer.

6. The integrated circuit of Claim 1 wherein the integrated circuit is a CMOS semiconductor.

7. The integrated circuit of Claim 1 wherein the high speed bus interface is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.

8. An integrated circuit to communicate information with a core chipset over a high speed bus, comprising:

means for bus interfacing to the core chipset through the high speed bus;

means for controlling a high speed mass data storage unit, the controlling means in communication with the bus interfacing means and the high speed mass data storage unit; and

means for network interfacing to a network port, the network interfacing means in communication with the bus interfacing means and the network port.

9. The integrated circuit of Claim 8 wherein the controlling means is a serial ATA host adapter.

10. The integrated circuit of Claim 8 wherein the controlling means controls the high speed mass data storage unit in response to a signal from the core chipset.

11. The integrated circuit of Claim 8 wherein the means for network controlling includes a high speed Ethernet controller having an operating speed of at least 1 Giga Bit per second.

12. The integrated circuit of Claim 11 wherein the high speed Ethernet controller includes a MAC layer and a physical layer.

13. The integrated circuit of Claim 8 wherein the integrated circuit is a CMOS semiconductor.

14. The integrated circuit of Claim 8 wherein the bus interfacing means is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.

15. A method of communicating information with a data storage unit and a network port, comprising:

providing, in a semiconductor circuit, a high speed bus interface to interface to a core chipset through a high speed bus;

providing a serial ATA host adapter in communication with the high speed bus interface to control the data storage unit in response to a signal from the core chipset; and

providing a high speed Ethernet network controller in communication with the high speed bus interface to control the network port.

16. The integrated circuit of Claim 15 wherein the serial mass data storage host adapter controls the high speed mass data storage unit in response to a signal from the core chipset.

17. The integrated circuit of Claim 15 wherein the network controller includes an Ethernet controller having an operating speed of at least 1 Giga Bit per second.

18. The integrated circuit of Claim 17 wherein the Ethernet controller includes a MAC layer and a physical layer.

19. The integrated circuit of Claim 15 wherein the high speed bus interface is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.

20. An integrated circuit to communicate information between a core chipset and a network port and a data storage unit over a high speed bus, comprising:

a high speed bus interface to interface to the core chipset through the high speed bus;

a serial ATA host adapter in communication with the high speed bus interface to control the data storage unit in response to a signal from the core chipset; and

a high speed Ethernet network controller in communication with the high speed bus interface to control the network port.

21. The integrated circuit of Claim 19 wherein the high speed bus interface is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.

22. The integrated circuit of Claim 19 wherein the high speed Ethernet controller has an operating speed of at least 1 Giga Bit per second.

23. The integrated circuit of Claim 22 wherein the high speed Ethernet controller includes a MAC layer and a physical layer.

24. An integrated circuit to communicate information between a core chipset and a network port and a data storage unit over a high speed bus, comprising:

means for bus interfacing to the core chipset through the high speed bus;

means for controlling the data storage unit, the controlling means to provide communication between the high speed bus interface and the data storage unit in response to a signal from the core chipset; and

means for network interfacing to a network port, the network interfacing means in communication with the high speed bus interface and the network port.

25. The integrated circuit of Claim 24 wherein the means for bus interfacing is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus

interface, a 3GIO bus interface, and an Infiniband bus interface.

26. The integrated circuit of Claim 24 wherein the network interfacing means includes an Ethernet controller having an operating speed of at least 1 Giga Bit per second.

27. The integrated circuit of Claim 26 wherein the Ethernet controller includes a MAC layer and a physical layer.

28. A multi-port integrated circuit to communicate information between a core chipset and at least two peripheral devices over a high speed bus, the two peripheral devices including a data storage unit and a network device, comprising:

a high speed bus interface to interface to the core chipset through the high speed bus;

a serial ATA host adapter in communication with the high speed bus interface and a first port to control the data storage unit in response to a signal from the core chipset; and

a high speed Ethernet network controller in communication with the high speed bus interface and a second port to control the network device.

29. The integrated circuit of Claim 28 wherein the high speed Ethernet network controller includes an Ethernet controller having an operating speed of at least 1 Giga Bit per second.

30. The integrated circuit of Claim 29 wherein the Ethernet controller includes a MAC layer and a physical layer.

31. The integrated circuit of Claim 28 wherein the high speed bus interface is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.

32. A multi-port integrated circuit to communicate information between a core chipset and at least two peripheral devices over a high speed bus, the two peripheral devices including a data storage unit and a network device, comprising:

means for bus interfacing to the core chipset through the high speed bus;

means for controlling the data storage unit in serial communication with the high speed bus interface and a first

port to control the data storage unit in response to a signal from the core chipset; and

means for network interfacing to a second port, the network interfacing means in communication with the high speed bus interface and the second port to control the network device.

33. The integrated circuit of Claim 32 wherein the network interfacing means includes an Ethernet controller having an operating speed of at least 1 Giga Bit per second.

34. The integrated circuit of Claim 33 wherein the Ethernet controller includes a MAC layer and a physical layer.

35. The integrated circuit of Claim 32 wherein the bus interfacing means is selected from the group comprising at least one of a PCI-X bus interface, a HyperTransport bus interface, a 3GIO bus interface, and an Infiniband bus interface.